QPL9065
Ultra Low-Noise 2-Stage Bypass LNA

Product Description

The QPL9065 is a high-linearity, ultra-low noise 2-stage gain block amplifier module with a bypass mode functionality integrated to the second stage in the product. At 1.95 GHz, the amplifier, under high gain mode, typically provides 37.5 dB gain, +36 dBm OIP3, and 0.55 dB noise figure while drawing 160 mA current from a +5 V supply. The component also provides high performance in the low gain mode with 17.5 dB gain, 0.55dB noise figure and +33 dBm OIP3 while drawing 70 mA current.

The QPL9065 uses a high performance E-pHEMT process. This low noise amplifier contains an internal active bias to maintain high performance over temperature.

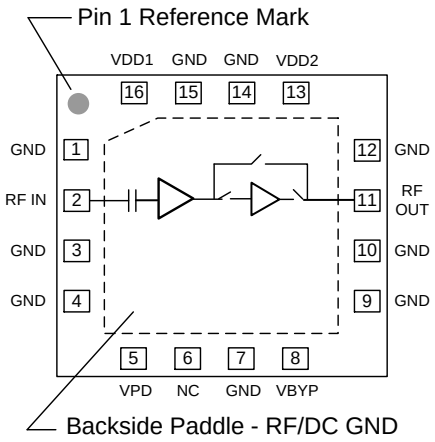
The QPL9065 covers the 0.45 – 3.8 GHz frequency band and is targeted for wireless infrastructure. The QPL9065 is housed in a 3.5 x 3.5 mm SMT package.

16 Pin 3.5 X 3.5 mm Leadless SMT Package

Product Features

- 0.45 – 3.8 GHz Operational bandwidth
- 2nd stage LNA with integrated bypass mode
- Ability to turn LNA and bypass mode OFF
- Ultra low noise, 0.55 dB at 1.95 GHz
- 37.5 dB Gain at 1.95 GHz, 17.5 dB in Low Gain Mode
- +36 dBm Output IP3 in High Gain Mode
- +33 dBm Output IP3 in Low Gain Mode
- Positive supply only, +3.3 to +5 V
- 1.8V CMOS TTL logic compatible on pins 5 & 8

Functional Block Diagram



Applications

- Base Station Receivers
- Tower Mount Amplifiers
- Repeaters
- FDD-LTE, TDD-LTE, WCDMA
- General Purpose Wireless

Ordering Information

Part No.	Description
QPL9065SR	100 pieces on a 7” reel
QPL9065TR13	2500 pieces on a 13” reel
QPL9065PCB401	1.7-2.7GHz Tuned Evaluation Board

Absolute Maximum Ratings

Parameter	Range / Value	Units
Storage Temperature	−65 to 150	°C
Drain Voltage (V_{DD})	+7	V
Input Power (CW)	+22	dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage	+3.3	+5.0	+5.25	V
T_{CASE}	−40		+105	°C
Tj at T_{CASE} max			+149	°C

Electrical specifications are measured under bias, signal and temperature conditions as specified. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp. = +25°C.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		450		3800	MHz
Test Frequency			1950		MHz
Gain	LNAs ON, Bypass OFF	35.5	37.5	39.5	dB
Input Return Loss	LNAs ON, Bypass OFF		12.5		dB
Output Return Loss	LNAs ON, Bypass OFF		15		dB
Noise Figure	LNAs ON, Bypass OFF		0.55	0.8	dB
Output P1dB	LNAs ON, Bypass OFF	+17.5(1)	+20.8		dBm
Output IP3	LNAs ON, Bypass OFF, Pout=+5 dBm/tone, Δf=1 MHz	+32	+36		dBm
Gain	LNA1 ON, Bypass ON		17.5		dB
Input Return Loss	LNA1 ON, Bypass ON		11.5		dB
Output Return Loss	LNA1 ON, Bypass ON		12		dB
Noise Figure	LNA1 ON, Bypass ON		0.55	0.8	dB
Output P1dB	LNA1 ON, Bypass ON		+18		dBm
Output IP3	LNA1 ON, Bypass ON, Pout=+5 dBm/tone, Δf=1 MHz	+30	+33		dBm
Control Voltage, V_{PD}, V_{BYP}	V_{IH}	1.17		3.3	V
	V_{IL}	0		0.63	V
Current, I_D	LNAs ON, Bypass OFF	80	160	200	mA
	LNA1 ON, LNA2 OFF, Bypass ON	43	70	98	mA
	LNAs OFF, Bypass OFF		5		mA
Thermal Resistance, θ_{jc}	High gain Mode (Channel to case)			42	°C/W
	Low gain Mode (Channel to case)			70	°C/W

Notes:
1. P1dB is not measured in production test. This min spec is calculated based on design confidence.

Control Truth Table

V_{PD}	V_{BYP}	State
1	0	LNA1 OFF, LNA2 OFF, Bypass OFF
0	0	LNA1 ON, LNA2 ON, Bypass OFF
0	1	LNA1 ON, LNA2 OFF, Bypass ON
1	1	LNA1 OFF, LNA2 OFF, Bypass ON

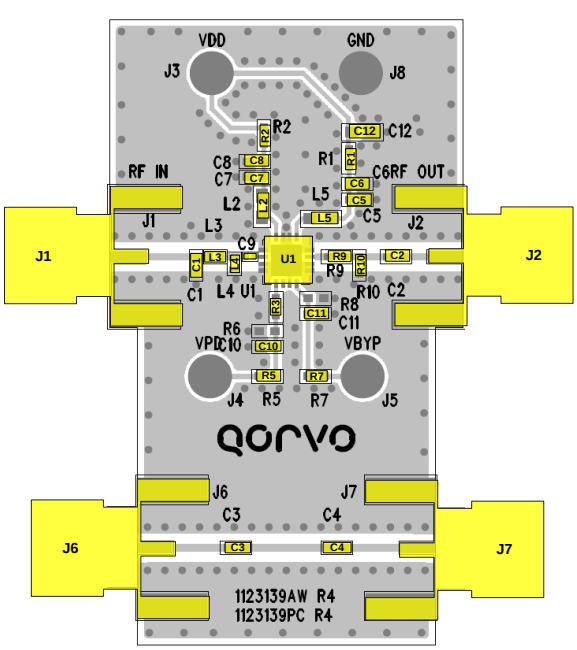
Switching Speed (1)

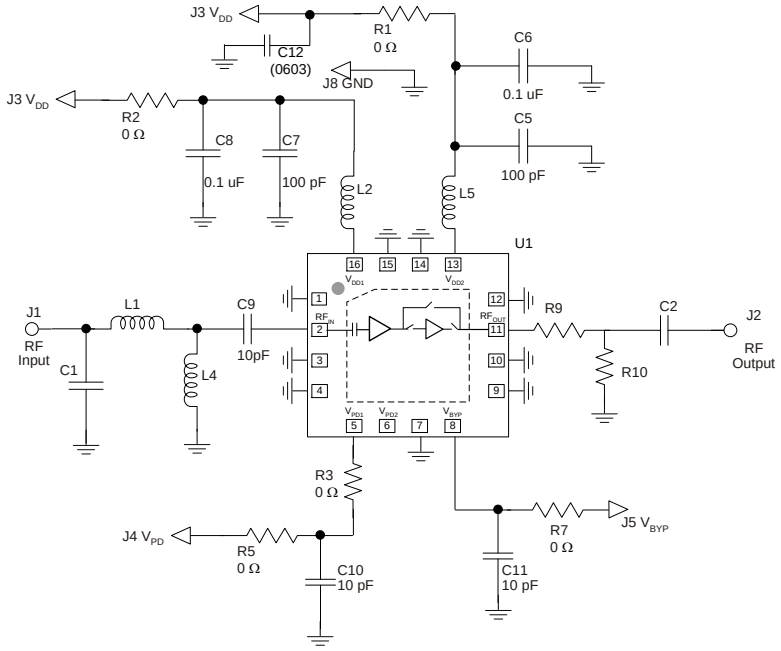
V_{PD}	V_{BYP}	State	50% of Vctrl to 90% of RF			50% of Vctrl to 10% of RF			Units
			-40 °C	25 °C	105 °C	-40 °C	25 °C	105 °C	
0	0	LNA1 ON, LNA2 ON, Bypass OFF	730	400	360	880	730	640	ns
1	1	LNA1 OFF, LNA2 OFF, Bypass ON							
0	0	LNA1 ON, LNA2 ON, Bypass OFF	276	292	300	780	740	690	
0	1	LNA1 ON, LNA2 OFF, Bypass ON							
1	1	LNA1 OFF, LNA2 OFF, Bypass ON	214	190	176	303	275	256	
0	1	LNA1 ON, LNA2 OFF, Bypass ON							

Note:

1. To achieve the fast switching speed listed, placement of R8 and C13 are critical. Refer to pg. 4 for EVB schematic and BOM.

QPL9065 Evaluation Board (1.7 – 2.7 GHz tuned)





See Evaluation Board PCB Information section for PCB material and stack-up.

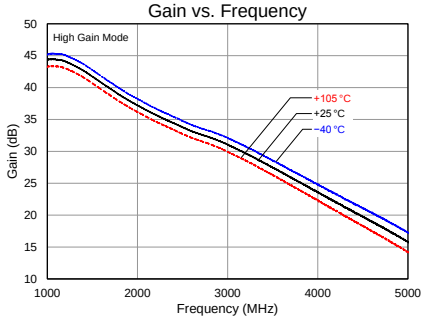
Bill of Material – QPL9065 Evaluation Board

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	PCB	Qorvo	1123139
U1	n/a	2-Stage Bypass LNA	Qorvo	QPL9065
R1, 2, 3, 5, 7	0 Ω	RES, 0402, +/-5%, 1/16W	Various	
R10	39K	RES, 0402, +/-5%, 1/16W	Various	
C1	0.5 pF	CAP, 0402, +/-0.1pF, 50V, C0G	Murata	GJM1555C1HR50BB01D
R9	5.1 Ω	RES, 0402, +/-5%, 1/16W	various	
L1	1.5 nH	IND, 0402, +/-0.1nH, 1000mA	Murata	LQP15MN1N5B02D
L4	6.8 nH	IND, 0402, +/-2%, 700mA	Murata	LQG15HS6N8J02
C2, 3, 4, 5, 7	100 pF	CAP, 0402, +/-5%, 50V	Various	
C6, 8	0.1 uF	CAP, 0402, 20%, 16V, Y5V	Various	
C9	10 pF	CAP, 0201, 2%, 50V	Murata	GRM0335C1H100GA01
C12	4.7 uF	CAP, 0603, 20%, 10V, Y5V	Various	
C10, 11	10 pF	CAP, 0402, 2%, 50V	various	
L2	2.2 nH	IND, 0402, +/-0.2nH, 1000mA	Murata	LQW15AN2N2C10
L5	18 nH	IND, 0603, 5%	Coilcraft	0603CS-18NXJL

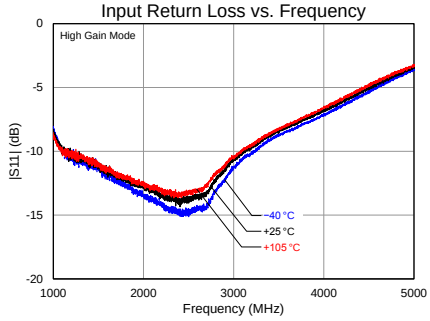
Performance Plots

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp.= +25 °C

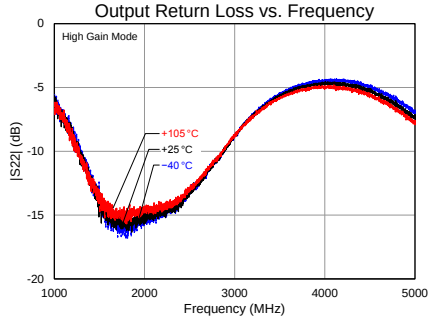
Gain vs. Frequency



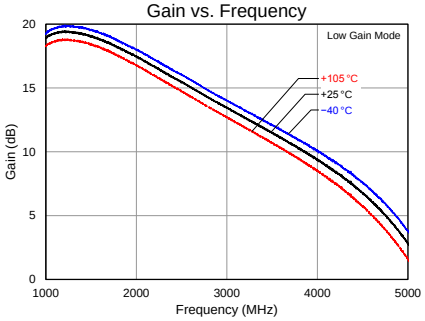
Input Return Loss vs. Frequency



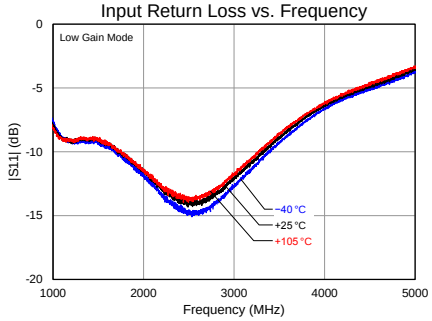
Output Return Loss vs. Frequency



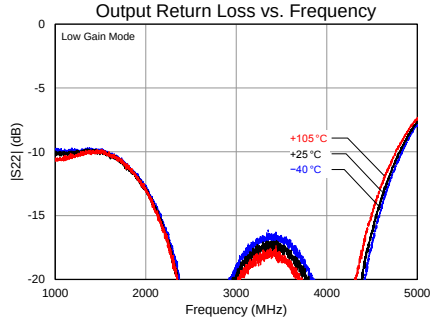
Gain vs. Frequency



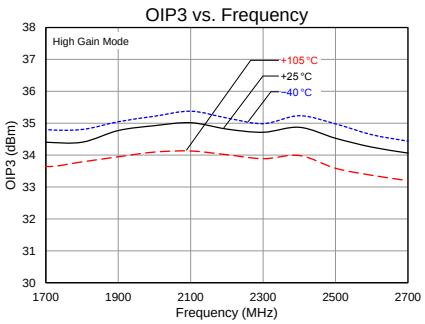
Input Return Loss vs. Frequency



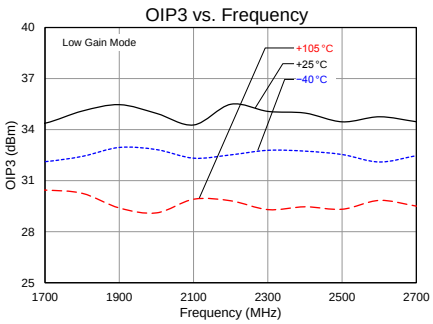
Output Return Loss vs. Frequency



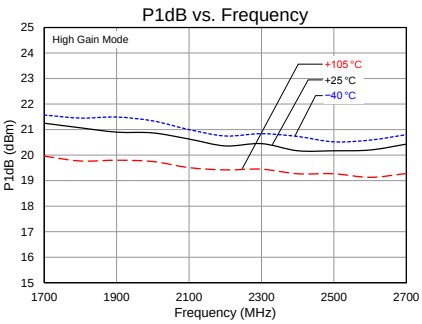
OIP3 vs. Frequency



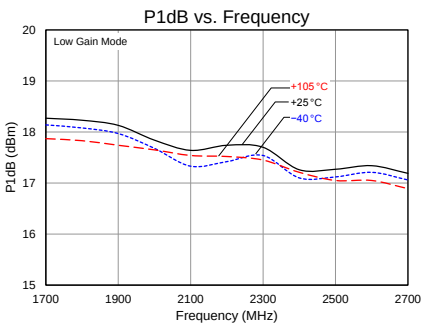
OIP3 vs. Frequency



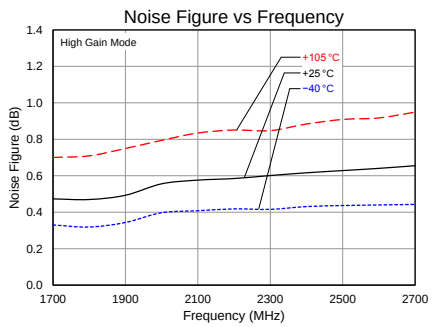
P1dB vs. Frequency



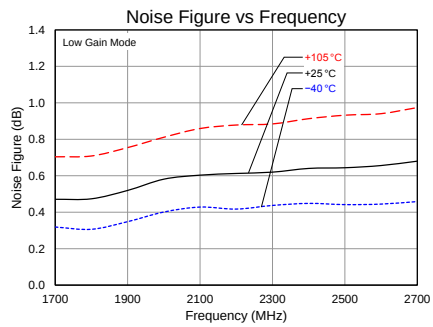
P1dB vs. Frequency



Noise Figure vs Frequency



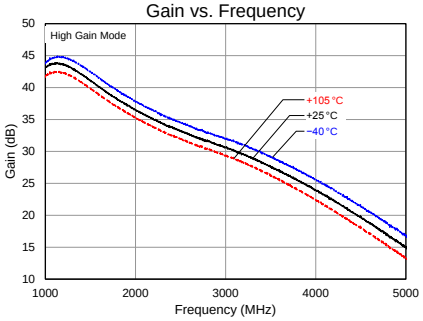
Noise Figure vs Frequency



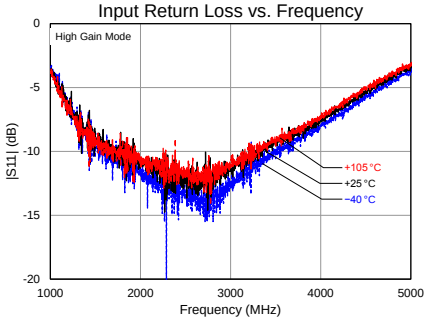
Performance Plots (V_{DD} = 3.3V)

Test conditions unless otherwise noted: V_{DD} = +3.3 V, I_{DD}(high gain mode) = 98mA, I_{DD}(low gain mode) = 55mA, Temp.= +25 °C

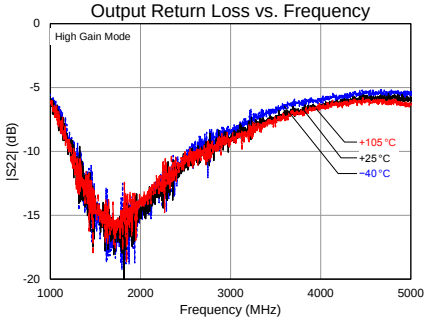
Gain vs. Frequency



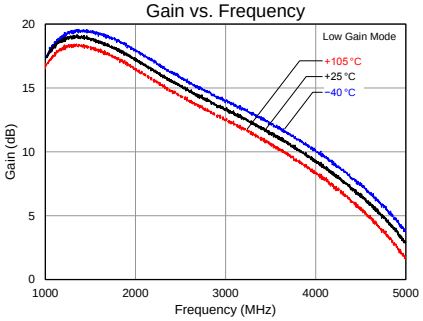
Input Return Loss vs. Frequency



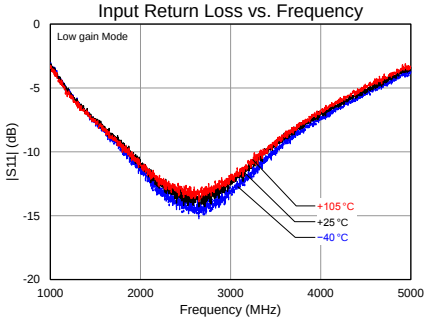
Output Return Loss vs. Frequency



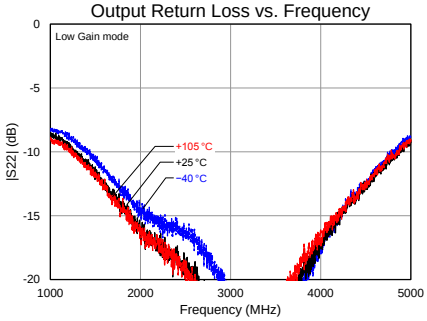
Gain vs. Frequency



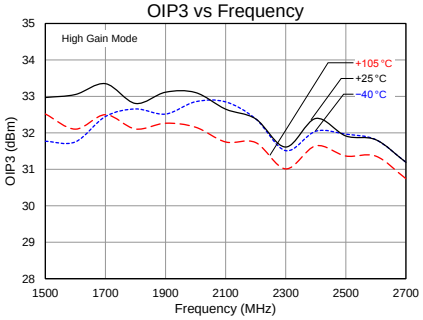
Input Return Loss vs. Frequency



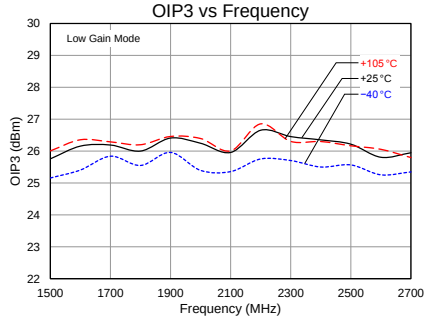
Output Return Loss vs. Frequency



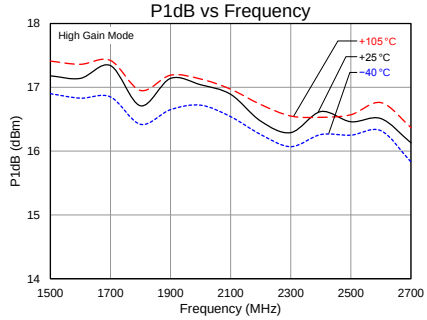
OIP3 vs Frequency



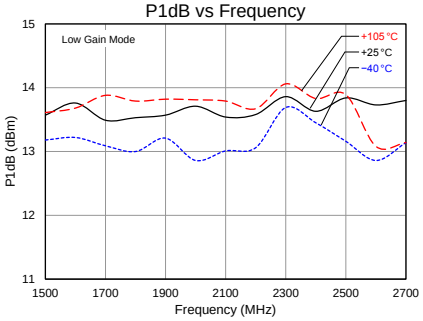
OIP3 vs Frequency



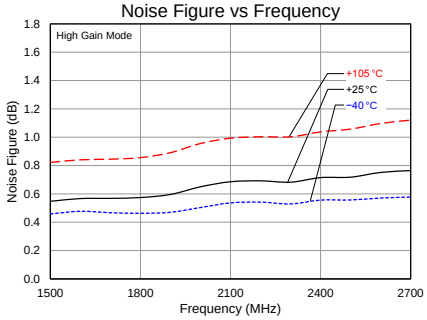
P1dB vs Frequency



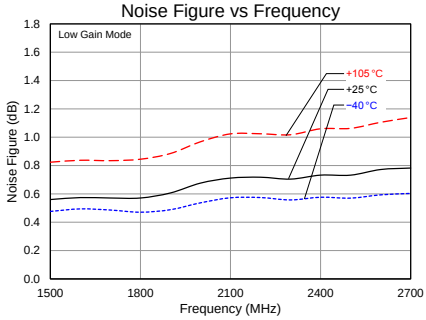
P1dB vs Frequency



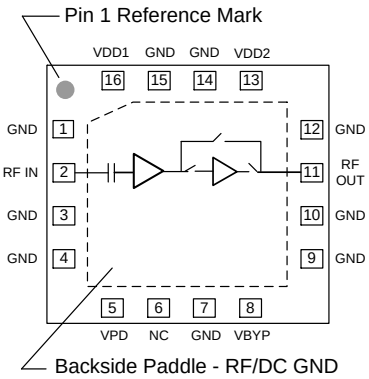
Noise Figure vs Frequency



Noise Figure vs Frequency



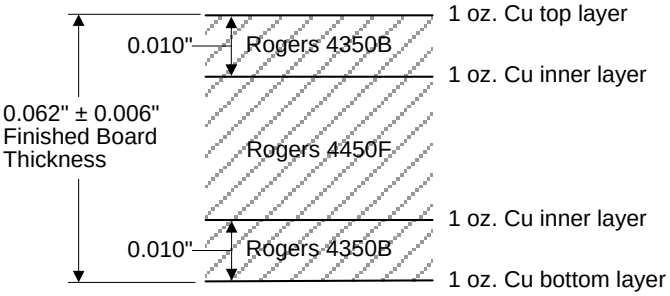
Pin Configuration and Description



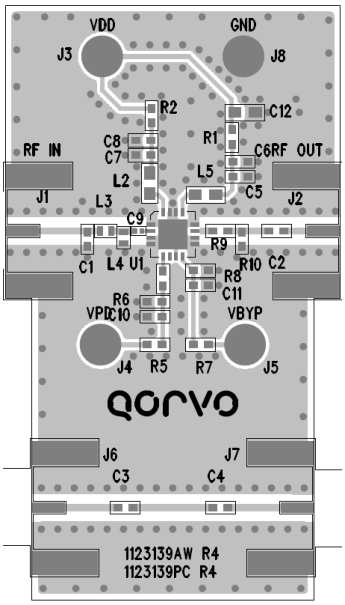
Pin No.	Label	Description
1,3,4,7,9,10,12,14,15	GND	RF/DC Ground pin.
2	RFin	RF input pin. Internally DC blocked.
5	V_{PD}	Power Down control for LNAs. Refer to truth table on pg. 2. Voltage should not exceed 3V. Recommended that VDD1 is applied before the control voltage.
6	NC	No internal connection but can be grounded for mounting integrity.
8	V_{BYP}	Bypass mode enable pin for LNA2. Refer to truth table on pg. 2. Voltage should not exceed 3V. Recommended that VDD1 is applied before the control voltage.
11	RFout	RF output pin. External DC block required.
13	V_{DD2}	Supply voltage pin for LNA2.
16	V_{DD1}	Supply voltage pin for LNA1.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

Evaluation Board PCB Information

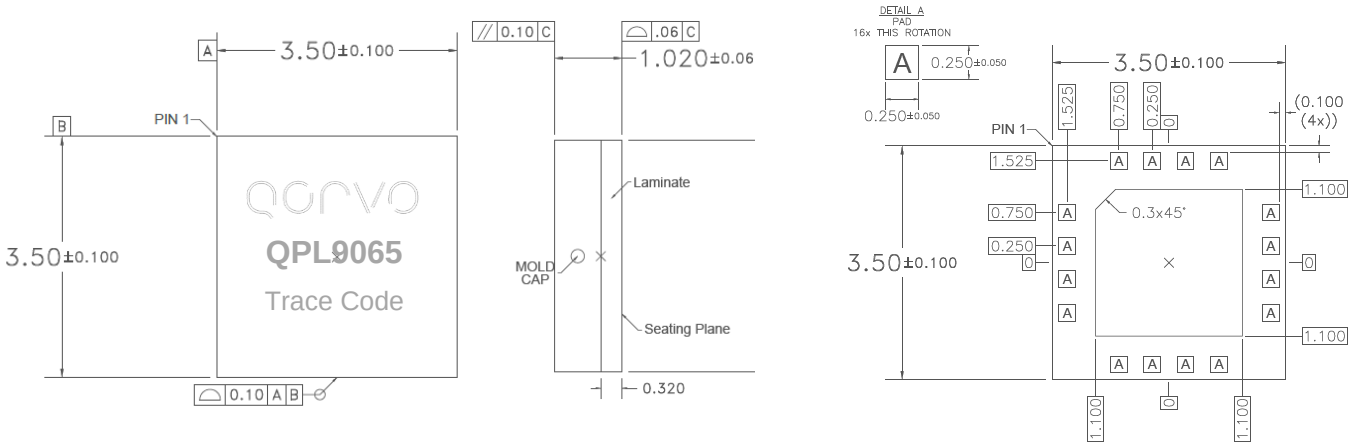
Qorvo PCB 1123139 Material and Stack-up



50 ohm line dimensions: width = .020”, spacing = .032”

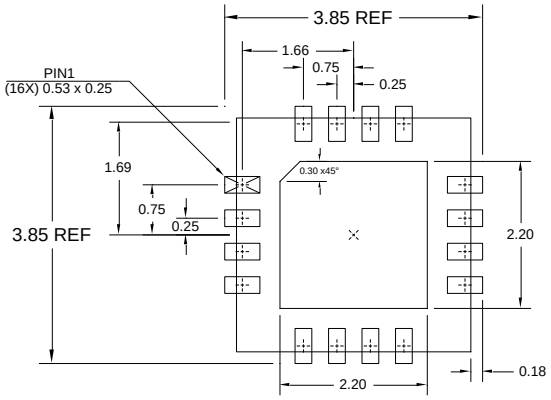


Package Marking and Dimensions

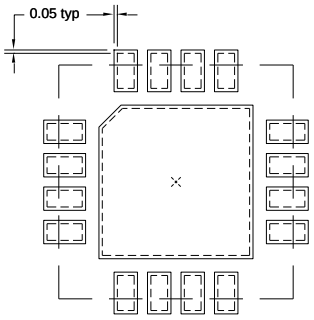


Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



RECOMMENDED
LAND PATTERN



RECOMMENDED
LAND PATTERN MASK

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation.
4. Do not remove or minimize via hole structure in the PCB. Thermal and RF grounding is critical.
5. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
6. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Electrolytic Plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Tel: 1-844-890-8163
Email: customer.support@qorvo.com

For technical questions and application information:

Email: sjcapplications.engineering@qorvo.com

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